PM8385

QuadPHY® RT

4-Port FC/GE Retimer

Revision A Device Errata

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1 Introduction

In this document:

- Section 2 lists the known functional errata for Revision A of the PM8385 QuadPHY RT.
- Section 3 lists documentation errors found in Issue 1 of the Data Sheet PMC-2031860.

1.1 Device Identification

The information contained in Section 2 relates to Revision A of the PM8385 Device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

Figure 1 - PM8385 QuadPHY RT Branding Format

1.2 References

1. Issue 1 of the PM8385 Data Sheet PMC-2031860, December 2003.
2 Device Functional Deficiency List

This section lists the known functional deficiencies for Revision A of the PM8385 device as of the publication date of this document.

Please report any functional deficiencies not covered in this errata to PMC-Sierra.
2.1 Incorrect default CRC in pattern generator

Description

The Custom Pattern CRC Registers 1 thru 4 (registers 0x11D, 0x11E, 0x11F, and 0x120) contain incorrect default values. As a result, when the custom pattern generator is selected to transmit the default pattern, a FC receiver (such as a FC tester, or another QuadPHY RT port’s Rx, when looped back to the Tx port under test) will detect CRC32 errors.

Workarounds

If the custom pattern generators default pattern is to be used, the values in the Custom Pattern CRC Registers 1 thru 4 (registers 0x11D, 0x11E, 0x11F, and 0x120) should be overwritten with 0x226, 0x371, 0x18E, and 0x2D8 respectively. In addition, the Custom Pattern EOF Registers 1 thru 4 (registers 0x121, 0x122, 0x123, and 0x124) should be overwritten with values 0x283, 0x155, 0x195, and 0x195 respectively.

Performance With Workaround

Normal operation.

Performance Without Workaround

Operation without workaround will cause a receiver connected to the Tx port configured for transmitting the default custom pattern to detect CRC32 errors.
2.2 Half Rate and Quarter Rate patterns are not generated correctly

Description

Table B.4 of the Jitter Working Group Technical Report Revision 10, June 9, 1999 -- T11.2 / Project 1230/ Rev 10 -Fibre Channel - Methodologies for Jitter Specification defines half rate and quarter rate patterns as follows:

Byte = D21.5 is repeated q times
Byte = D24.3 is repeated q times,
Byte = D10.2 is repeated q times,
Byte = D25.6, D6.1 is repeated q times,
Byte = D6.1, D25.6 is repeated q times,

where “q” can be chosen as any value.

In the PM8385 QuadPHY RT device, the half rate and quarter rate patterns are generated as follows:

Byte = D21.5 is repeated 8 times,
Byte = D24.3 is repeated 8 times,
Byte = D10.2 is repeated 8 times,
Byte = D25.6, D6.1 is repeated 4 times,
Byte = D6.1, D25.6 is repeated 4 times.

Workarounds

If half rate and quarter rate pattern generation is required, the custom pattern generator registers can be used as follows (value 4 is used for “q”):

- program D21.5 (0x0155) into Custom Pattern SOF Registers 1 to 4 (0x111 to 0x114),
- program D24.3 for negative current running disparity (0x0333) into Custom Pattern DATA1 Registers 1 and 3 (0x115 and 0x117),
- program D24.3 for positive current running disparity (0x00cc) into Custom Pattern DATA1 Registers 2 and 4 (0x116 and 0x118),
- program D10.2 (0x02aa) into Custom Pattern DATA2 Registers 1 to 4 (0x119 to 0x11C),
- program D25.6 (0x0199) into Custom Pattern CRC Registers 1 and 3 (0x11D and 0x11F),
- program D06.1 (0x0266) into Custom Pattern CRC Registers 2 and 4 (0x11E and 0x120),

- program D25.6 (0x0199) into Custom Pattern EOF Registers 1 and 3 (0x121 and 0x123),

- program D06.1 (0x0266) into Custom Pattern EOF Registers 2 and 4 (0x122 and 0x124),

- program D06.1 (0x0266) into Custom Pattern Idle Registers 1 and 3 (0x125 and 0x127),

- program D25.6 (0x0199) into Custom Pattern Idle Registers 2 and 4 (0x126 and 0x128),

- program hex value 0x0082 into Custom Pattern Control Register (0x110); this will configure the pattern generator to repeat the DATA1 and DATA2 patterns only once, and the Idle pattern twice.

After the above registers are programmed, the half rate and quarter rate pattern generation may be enabled by setting the "En Pattern Generator" bit in Pattern Generator/Comparator Control Register (0x10F) to logic 1.

**Performance with Workaround**

FC compliant half rate and quarter rate patterns can be generated by programming the custom pattern generator as described in the Workarounds section above.

**Performance without Workaround**

The half rate and quarter rate pattern generated by the PM8385 QuadPHY RT device is not compliant to the FC specifications.
2.3 LCV threshold[15:0] of 0xXXFF will disable LCV rate interrupt generation and 0xFFFF will disable LCV rate and absolute interrupt generation

Description

Setting LCV Threshold[15:0] bits (register 0x00B) to 0xXXFF will disable LCV rate interrupt generation. Setting LCV Threshold[15:0] to 0xFFFF will disable both LCV rate and LCV absolute interrupts generation.

Workarounds

If interrupt generation based on LCV rate count is desired, the LCV Threshold[15:0] bits should not be set to 0xXXFF. If interrupt generation based on LCV absolute count is desired, the LCV Threshold[15:0] bits should not be set to 0xFFFF.

Performance With Workaround

Normal operation.

Performance Without Workaround

Interrupt generation based on rate and/or absolute LCV counts will be disabled.
2.4 **CRC32 threshold[15:0] of 0xXXFF will disable CRC32 rate interrupt generation and 0xFFFF will disable CRC32 rate and absolute interrupt generation**

**Description**

Setting CRC32 Threshold[15:0] bits (register 0x00C) to 0xXXFF will disable CRC32 rate interrupt generation. Setting CRC32 Threshold[15:0] to 0xFFFF will disable both CRC32 rate and CRC32 absolute interrupts generation.

**Workarounds**

If interrupt generation based on CRC32 rate count is desired, the CRC32 Threshold[15:0] bits should not be set to 0xXXFF. If interrupt generation based on CRC32 absolute count is desired, the CRC32 Threshold[15:0] bits should not be set to 0xFFFF.

**Performance With Workaround**

Normal operation.

**Performance Without Workaround**

Interrupt generation based on rate and/or absolute CRC32 counts will be disabled.
3 Documentation Deficiency List

There are no known documentation deficiencies for Issue 1 of the PM8385 Data Sheet PMC-2032005 as of the publication date of this document.

Please report any documentation deficiencies not covered in this errata to PMC-Sierra.