OVERVIEW

The ClassiPI™ family provides the cornerstone for building content and policy-based network equipment. It enables analysis and classification for all layers of a packet, including payload, at wire speeds from 100Mb/s to Gigabit LANs, as well as OC48 and higher speeds WANS.

ClassiPI offloads packet identification and classification from the network processor, freeing it to handle its traditional editing and forwarding functions. ClassiPI’s architecture allows easy scaling of the number of policies and performance, making it ideally suited for enterprise, service provider and carrier edge equipment.

The ClassiPI PM2329 is the latest member in the ClassiPI™ family of network classification processors optimized for complex packet classification and analysis.

Classification and analysis capabilities can provide hardware acceleration to implement wire-speed routing, Quality of Service (QoS), firewall and other functionality such as Network Address Translation (NAT) and intrusion detection at OC48 speeds.

FEATURES

- Advanced layer 2 through layer 7 content matching capabilities
- Gluelessly interfaces with many network processors using synchronous SRAM (ZBT or Sync Burst) bus operating up to 6.4 Gbps. System interface supports DMA mode for data transfer
- Supports 8Kbyte maximum packet size
- Classification and analysis up to OC48 speed using header, payload or user-defined data
- Key length programmable from 1 to 192 bytes
- Provides 16K policy database entries with one classification processor and 128K entries with eight classification processors
- Performs forward and reverse content searches
- Policy database configurable into multiple partitions with each partition storing a different class of rules
- Searches executed sequentially, conditionally and/or in parallel using sophisticated chaining mechanisms
- Supports up to 32 independent input/output request/response data channels
- Interfaces to an optional SSRAM for extended capabilities such as programmed search sequencing, per rule statistics collections, timestamp, and user data.
- IPv4 aware and IPv6 ready

APPLICATIONS

- Content-based Switches
- Access Concentrators
- Intrusion Detection Systems
- Firewalls
- Switches
- Routers
- Load Balancers
- Traffic Shapers
- Bandwidth Management Platforms
- Network Address Translators

In each application, the PM2329 accelerates a variety of functions, such as address lookup, flow classification, and connection cache identification. The result of these lookups or classifications is returned as a series of indexes or tags.

System designers can attach an optional external SSRAM to the PM2329 that can store user programmable data corresponding to the indexes that are returned upon a match.

DESCRIPTION

The PM2329 is Ethernet (II, 802.3, 802.1p,q) IP, TCP/UDP aware and incorporates an engine that extracts key IP, TCP and UDP header fields as well as payload data at any offset. System designers can choose to bypass the extraction engine on a per packet basis.

The PM2329 has the unique ability to perform a sequence of classifications, allowing a hardware implementation of if-then-else logic. This enables the system designer to completely off-load complex packet processing decision trees to the PM2329 processor.

The PM2329’s high-speed wide synchronous data transfer bus optimizes data transfers. Operating at 50/66/100 MHz, the 32/64-bit bus provides adequate bandwidth to transfer data, commands, and results supporting rates greater than OC48.

The PM2329’s internal search engines can be set to operate at up to 200MHz irrespective of the system interface speed, ensuring that performance does not degrade due to slower system components.
The PM2329's flexible system interface architecture allows complete hardware controlled data transfer for high-speed applications, as well as network-processor-driven software control. The PM2329 can be configured to receive streaming commands and data through its system interface. Content can consist of:

- arbitrary bytes
- partial IP packets (IP header, TCP header, or partial data), or
- complete IP packets.

The data is preceded by command words that identify the nature of the data following immediately, as well as the kinds of classification to be performed, thus ensuring high-speed command and data input and efficient use of the system interface. Under the external network processor's control, the ClassiPI PM2329 can optionally execute multiple commands on the same packet.

The PM2329 network classification processor is capable of performing:

- connection state maintenance
- single or multiple match identification
- prioritized match selection on multiple matches
- range matches on multiple key fields
- regular expression content searches – case insensitive strings, numbers and other content
- timestamp support
- counters / statistics (packet and byte count)
- dynamic rule update support
- conditional search sequencing

**PM2329 MAJOR BLOCKS**

**Extraction Engine**

The extraction engine (EE) performs Ethernet (II, 802.3, 802.1p,q) IP, TCP and UDP header analysis and creates a header key made up of typical L3 addresses and L4 port number fields. The EE enables data payload-based classification by extracting user-defined keys from any location within the packet's payload. The EE can optionally maintain partial TCP state information in external SSRAM. Where IP/TCP/UCP header extraction is done outside the PM2329, header parsing can be disabled.

**Rule Processing Engine**

The rule processing engine (RPE) stores each entry in a policy database as a rule made up of an Op-code and corresponding operand data. 16K rules reside in RAM internal to the RPE.

The RPE applies multiple rules to the supplied data and determines the entry that results in a match. If multiple rules result in a match, the RPE uses a built-in prioritization mechanism to identify a unique rule entry. Up to four consecutive rules can be combined to form a composite rule.

**Operation Cycle Scheduler**

The operation cycle scheduler (OCS) autonomously classifies packets by selectively applying user-defined rules/policies on a packet, and returns the results to the network processor.

The OCS executes an operation cycle (OC) by fetching a predefined set of rules from on-chip memory and applying them to a packet. OCs can execute sequentially or conditionally, using external RAM, via fully programmable C-like logical constructs such as if-then-else and switch-case.

To reduce development time and accelerate time-to-market, the PM2329 provides robust trace/debug features to assist the system designer in code debug.

The OCS also provides a processor controlled sequencing feature, allowing the network processor to augment packet classification and analysis. More than four OCs can execute on a single packet, which is useful for complex packet analysis.

**Extended Policy, Control and Statistics Interface**

An optional external SSRAM, which can contain control and data information as well as traffic statistics, can be attached to the PM2329 processor. The PM2329 can execute operation cycles based on a powerful flow control mechanism driven by control words stored in this external SSRAM. Besides control words, the external SSRAM also contains user configurable data that can be included in the returned results. The PM2329 automatically updates statistical and TCP state information in the external SSRAM.

**PM2329 SYSTEM DIAGRAM**

The system diagram illustrates a typical application of the PM2329 processor within a line interface card for a high performance switch.