MSP8120

Multi-service Security Processor

Released Product Brief

PRODUCT OVERVIEW

PMC-Sierra's MSP8120 Multi-service Security-enabled processor is designed to meet the needs of networking, security appliances, and network attached storage applications.

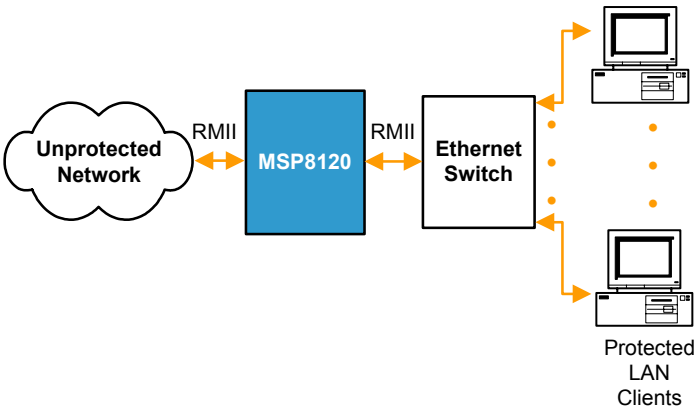
The MSP8120 integrates standards-based security hardware to accelerate internet protocol security (IPSec) and secure socket layer (SSL) performance for security appliances, firewalls, networking, and storage applications.

The MSP8120 is part of the MSP8100 Series of highly-integrated, feature-rich products that incorporate the high performance, power-efficient MIPS 34K core. The processor provides PCI, dual Ethernet, ROM, Flash, DDR, and low-speed peripheral interfaces, which are connected internally to the MIPS 34K core by a high-bandwidth multi-service bus.

BENEFITS

- High-performance 400 MHz MIPS32 core enables demanding packet processing and network security applications
- Highly integrated system-on-a-chip (SoC) solution simplifies board design, reducing component and overall system cost
- Hardware IPSec processing frees up the CPU for other applications
- Optimized memory controller provides low latency, high bandwith access to SDRAM (333 MHz DDR-2)

MSP8120 NETWORK SECURITY APPLICATION



PRODUCT HIGHLIGHTS

INTEGRATED SECURITY SUBSYSTEM

- Integrated security subsystem:
- Dedicated 2-channel DMA controller for security packet processing
- IPSec engine:
  - Supports all IPSec packet transforms and implements SSL packet transforms
  - Implements DES/3DES/AES crypto and SHA-1/MD-5 hash algorithm support
- Integrated queue manager for intelligent buffer management
- Random number generator

MIPS 34K MICROPROCESSOR CORE

- Supports MIPS32 Release 2 instruction set
- 400 MHz operation
- 9-stage pipeline
- 64 Kbyte Instruction and Data caches
- MIPS16e Code Compression
- 32-bit address paths, 64-bit data paths to caches and external interface
- DSP instruction set extensions
- EJTAG debug and off-chip trace support

PROGRAMMABLE MEMORY MANAGEMENT UNIT

- 8-entry Instruction TLB (ITLB) and Data TLB (DTLB)
- 32 dual-entry Joint TLB (JTLB)
- JTLBs are sharable under software control

USB 2.0 CONTROLLER AND PHY

- Both host and device mode of operation
- Supports low-speed (LS) operation (1.5 Mbit/s), full-speed (FS) operation (12 Mbit/s) and hi-speed (HS) operation (480 Mbit/s)

SYSTEM INTERRUPT CONTROLLER

- Handles interrupts for on-chip peripherals and 8 external interrupts
- Supports up to 32 PCI message signaled interrupts (MSI)

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HIGH PERFORMANCE MULTI-SERVICE BUS (MS BUS) ARCHITECTURE

- 32 bits at 166 MHz (5.33 Gbit/s)
- DMA engines integrated for the Ethernet MACs, USB, TDM interface, security engine, and block copy engine

SYSTEM LOGIC AND PERIPHERALS MODULE

- 3.3 V PCI Local Bus 2.3-compliant host interface
- Configurable external Local Bus interface that supports data transfers up to 25 Mbytes per second
- Glueless interface to x8 Flash memories
- Clock manager and boot controller
- Serial Peripheral Interface/ Microprocessor Peripheral Interface (SPI/MPI)
- Two-Wire serial interface
- 20 GPIO pins
- System interrupt controller (internal and external interrupts)
- Two external timers / clock generator
- Two universal asynchronous serial (UART) interfaces

CLOCK MANAGER AND BOOT CONTROLLER

- In single crystal mode, all on-chip clocks are generated from a single 36 MHz crystal

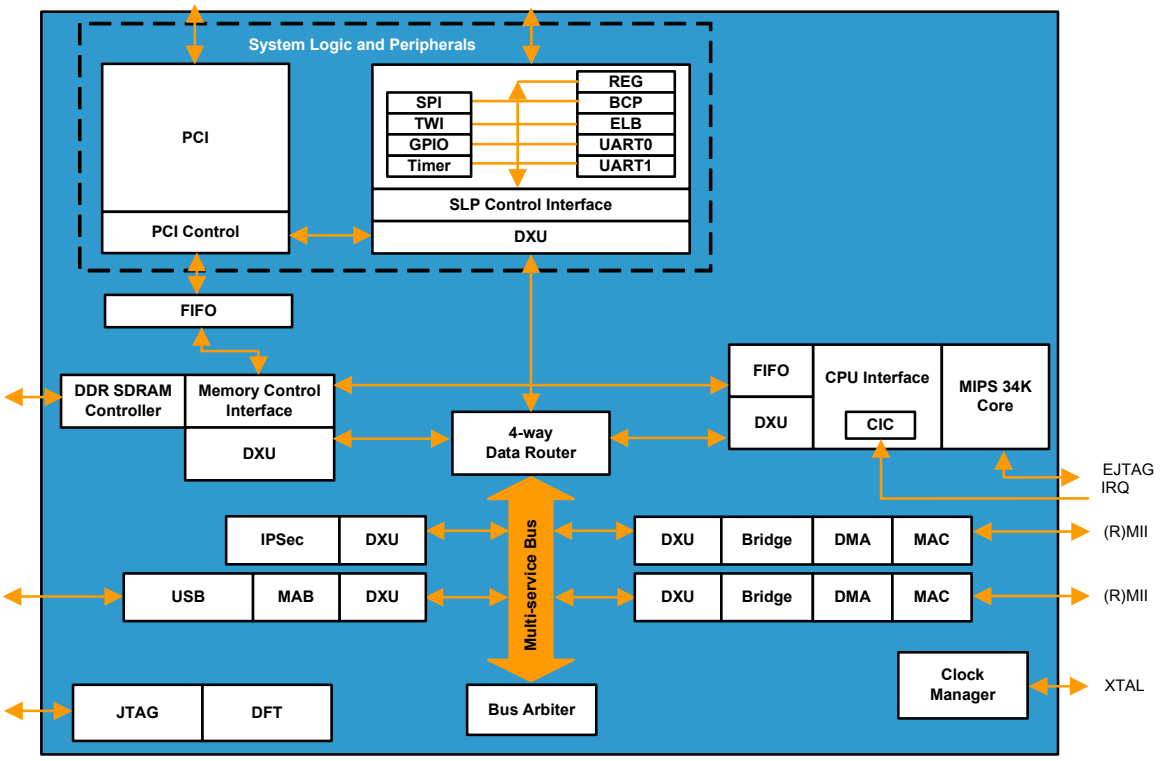
ETHERNET INTERFACE

- Two independent 10/100 Ethernet MAC controllers
- User selectable Media-Independent Interface (MII) or RMII (Reduced MII) Interface on each MAC

APPLICATIONS

- Security appliances
- Firewalls
- Networking applications
- Storage applications

BLOCK DIAGRAM



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All product documentation is available on our web site at: www.pmc-sierra.com.

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